

REMARKS/ARGUMENTS

Claims 1-3, 5, and 8 are pending in this application.

Claims 1-8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Shimizu (U.S. 5,834,345) or, in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Shimizu in view of Robertson et al. (EP 1 154 036). Applicant notes that Claims 4, 6, and 7 were canceled in the Amendment filed on November 21, 2007. Accordingly, the Examiner has clearly inadvertently listed Claims 4, 6, and 7 in the prior art rejection, and should have listed only Claims 1-3, 5, and 8. Applicant respectfully traverses the rejections of Claims 1-3, 5, and 8.

Claim 1 recites:

A transistor comprising:
a source electrode and a drain electrode arranged in mutually opposing relation;
a semiconductor film comprising at least one layer disposed between the source electrode and the drain electrode;
a gate electrode disposed in adjacent relation to the semiconductor film; and
a gate insulating film disposed between the gate electrode and each of the source electrode, the drain electrode, and the semiconductor film, wherein
a concentration of fluorine contained in the gate insulating film is 1×10^{20} atoms/cm³ or less;
the transistor is of an inverted stagger type in which the gate insulating film and the semiconductor film are formed in that order and the semiconductor film is disposed on the gate insulating film; and
the gate insulating film is an amorphous silicon nitride film.
(emphasis added)

The Examiner alleged that Shimizu teaches all of the features recited in Applicant's Claim 1, including a gate insulating film that does not contain a concentration of fluorine which would read on the feature of "a concentration of fluorine contained in the gate insulating film is 1×10^{20} atoms/cm³ or less" as recited in Applicant's Claim 1. Alternatively, the Examiner alleged, "Robertson [et al.] teaches cleaning the CVD chamber using fluorine and thereafter completely removing fluorine

residue and particulates from the CVD chamber (par. 5-11 and 23)." Thus, the Examiner concluded that it would have been obvious "to clean the CVD apparatus of Shimizu with the method taught by Robertson [et al.] thus removing fluorine from being present in the amorphous silicon nitride." Applicant respectfully disagrees.

Contrary to the Examiner's allegations, neither Shimizu nor Robertson et al. teaches or suggests anything at all about a specific concentration of fluorine in a gate insulating film, and certainly fails to teach or suggest the feature of "a concentration of fluorine contained in the gate insulating film is 1×10^{20} atoms/cm³ or less" as recited in Applicant's Claim 1.

As disclosed in paragraph [0006] of Robertson et al., during the manufacture of semiconductor devices, such as FET thin film transistors, "the CVD chamber **must** be periodically cleaned to remove particulates between depositions. Cleaning is generally done by passing an etch gas, particularly a fluorine-containing gas, such as nitrogen trifluoride, into the chamber" (emphasis added). Thus, during the process of manufacturing the FET thin film transistor of Shimizu, the CVD chamber must be cleaned using a fluorine-containing gas. Since Shimizu fails to teach or suggest any special steps which could or should be taken to remove the fluorine from the CVD chamber prior to the gate insulating film 3 being formed, the gate insulating film of Shimizu would inherently contain a concentration of fluorine.

In addition, contrary to the Examiner's allegations, Robertson et al. fails to teach or suggest that the fluorine residue is completely removed from the CVD chamber. In fact, the cleaning method disclosed in Robertson et al. is substantially the same as the conventional cleaning method disclosed in paragraphs [0023] and [0024] of the present application, i.e., fluorine is passed into the CVD chamber where it reacts with unwanted deposits and particles, and then a hydrogen plasma process is performed to react with the fluorine to remove the fluorine from the CVD chamber (see, paragraph [0010] of Robertson et al.). However, as disclosed in paragraphs [0023] and [0024] of the present application, conventional CVD apparatuses, such as the CVD apparatus

disclosed in Robertson et al., include an anode having a surface thereof which is composed of an anodic oxidation protective film which is porous. Since the anodic oxidation protective film of the anode is porous, fluorine is trapped in the pores in the anodic oxidation protective film, and the fluorine cannot be completely removed by the hydrogen plasma process of Robertson et al. Thus, after the cleaning method disclosed in Robertson et al., fluorine is still present in the CVD chamber.

The inventors of the present application have determined that, by using the conventional cleaning method in a conventional CVD apparatus as disclosed in paragraphs [0023] and [0024] of the present application, the concentration of fluorine contained in the gate insulating film could not be reduced to less than about 3×10^{20} atoms/cm³. Since the cleaning method of Robertson et al. and the CVD chamber of Shimizu are substantially the same as those disclosed in paragraphs [0023] and [0024] of the present invention, if the cleaning method of Robertson et al. were used to clean the CVD chamber of Shimizu, then the concentration of fluorine contained in the gate insulating film of Shimizu would be expected to be about 3×10^{20} atoms/cm³ or more. Thus, the best result that the cleaning method of Robertson et al. and the CVD chamber of Shimizu could achieve is a concentration of fluorine of about 3×10^{20} atoms/cm³ or greater. Even if Robertson et al. and Shimizu could be combined, it would not enable a reduction in the concentration of fluorine below 3×10^{20} atoms/cm³.

Furthermore, contrary to the Examiner's allegations, it would not have been obvious to clean the CVD apparatus of Shimizu with the method taught by Robertson et al. Lines 15-17 of col. 8 of Shimizu teach, "According to the fabricating method of field effect thin film transistor, the fabrication steps become simple and the total fabrication cost is reduced." Robertson et al. teaches a complicated 5-step cleaning process. If the cleaning method of Robertson et al. was used to clean the CVD apparatus of Shimizu, the fabricating method of Shimizu would be significantly more complicated, and as a result, the total fabricating cost would be significantly increased. Therefore, contrary to the Examiner's allegations, one of ordinary skill in the art would not have

been motivated to combine the alleged teachings of Robertson et al. with the alleged teachings of Shimizu.

Thus, contrary to the Examiner's allegations, the combination of Shimizu and Robertson et al. fails to teach or suggest the feature of "a concentration of fluorine contained in the gate insulating film is 1×10^{20} atoms/cm³ or less" as recited in Applicant's Claim 1.

Accordingly, Applicant respectfully submits that Shimizu and Robertson et al., applied alone or in combination, fail to teach or suggest the features recited in Applicant's Claim 1.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 1 under 35 U.S.C. § 102(b) as being anticipated by Shimizu or, in the alternative, under 35 U.S.C. § 103(a) as being unpatentable over Shimizu in view of Robertson et al.

In view of the foregoing remarks, Applicant respectfully submits that Claim 1 is allowable. Claims 2, 3, 5, and 8 depend upon Claim 1, and are therefore allowable for at least the reasons that Claim 1 is allowable.

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

Application No. 10/595,640
May 5, 2008
Reply to the Office Action dated February 5, 2008
Page 8 of 8

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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